COEN 171 Design Project 3

Due: Friday, May 1, 2009

1. Introduction and Objectives

The goal of this project is to design and implement the datapath and control unit for a subset of the MIPS instruction set architecture. The circuit elements should be created using the Xilinx ISE design tools. You will be required to calculate the performance of your implementation in terms of execution time for a specified workload.

For this project, you are required to work in groups of four. You will lose 50% of the possible points on the project if you don't have a team of four. There may be a need for a team of 3 or five, but you must have my permission to have such a team size. Different groups may not work together, or discuss any details of their designs. You are encouraged to discuss any problems with the instructor or teaching assistant.

2. The Instruction Set Architecture

We will implement a subset of the MIPS 32-bit ISA, consisting of the following instructions:

R-Type:	ADD, SUB, AND, OR, SLT
I-Type:	ADDI, ORI, LUI, LW, SW, BEQ
J-Type	JAL, JR

3. Technology Specifications and Performance Evaluation

Implement the complete datapath and control unit for the above MIPS microprocessor unit, and verify that it properly executes all instructions. The technology that you are to use is the Virtex XCV100 field programmable gate array (FPGA), using Xilinx ISE software design tools and simulation tools to implement, simulate, verify, and evaluate your design.

It is your task to identify the clock speed and average cycles per instruction (CPI) at which your design can operate and to design a verification process that demonstrates consistent successful operation of each instruction type at that speed. Because behavioral simulations do not produce exact timing results, you will need to do an analysis of your design by hand. Depending on your implementation (single cycle, multi-cycle, pipelined), this will likely require a detailed critical path analysis for the overall design or for each type of instruction. You should assume 1ns per gate delays and use the following instruction count breakdown to determine average CPI:

Instruction	Frequency
R-Type	40%
ADDI, ORI	4%
LUI	2%
LW	20%
SW	20%
BEQ	10%
JAL	2%
JR	2%

The performance section of your report should provide the average CPI, the clock speed, and the time to execute a synthetic workload of 10^9 instructions.

4. What to turn in

Your report should be a complete description of all design, implementation, and verification activities. Turn in all electronic files (including a soft copy of the final report) in a single zipped file via blackboard. The report should include:

1. Introduction and Executive Summary, including specifics on which instructions have been successfully simulated, final performance figures and bonus eligibility.
2. Discussion of your design decisions and processes.
3. Your datapath design methods, including key schematics.
4. Your control unit design methods, including key schematics.
5. Testing and verification of final design components, including simulation plots.
6. Performance results of your design on the given workload.
7. Discussion and conclusions

5. Peer Review

Each person on your team will complete and submit a peer review form for their team, evaluating each team member's contribution. Peer review scores will be multiplied times the final team score to determine individual grades.

6. Bonus Structure

The incentive structure includes *simulation bonuses*, *architecture bonuses*, and *instruction bonuses*, as outlined below.

Simulation Bonuses:

- 5 point simulation bonus: Pre-load the instruction memory with a short sequence of instructions (minimum 10), and do a single simulation of the sequence, verifying all instructions execute properly. Include multiple instruction types within this sequence.
- 10 point simulation bonus: Write the program from Project 1 using only your implemented instructions, pre-load the memory with the machine code and an array of data, and simulate the execution of the program, verifying that the correct sorted data is placed into memory as specified. You may use hard-coded memory addresses for the data arrays.

Architecture Bonuses:

- 10 point multi-cycle architecture bonus: Implement and successfully simulate a multi-cycle datapath and control unit.
- 30 point pipelining architecture bonus: Implement and successfully simulate a pipelined datapath and control unit, including any necessary forwarding and stall hardware.

Instruction Bonuses:

- 0-5 points per additional instruction successfully implemented, depending on the complexity of the instruction (similar instructions requiring the same datapath modifications will receive bonus points as a group).
- 5 point performance bonus to the design team with successful simulation of the highest total number of unique instructions.